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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/578,440	05/25/2000	Hajime Washio	49855(904)	6115

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EXAMINER
ABDULSELAM, ABBAS I

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/578,440	WASHIO ET AL.	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 08/07/02 have been fully considered but they are not persuasive.

Applicant argues that Moriyama et al. (USPN 6232945) and Ishii (USPN 6081131) do not teach flip-flops of multiple steps that output in synchronization with a clock signal. Applicant also argues that Moriyama and Ishii do not disclose a plurality flip flops configured in a shift register for transmitting input pulse in synchronization with a clock signal and output a signal. However as will be shown in the art rejection below, Moriyama teaches a shift register circuit (21) including flip flops. Moriyama teaches that when a start pulse is inputted to the flip-flop 22 sub. 1, that start pulse is transferred to the succeeding stage flip-flop 22 sub 22 in synchronism with a clock pulse and output to the next step, which transmits it to the input stage switching circuit (23). See col. 15, lines 1-18 and Fig 4. Ishii teaches a horizontal system driver (48), vertical system driver (vertical shift register), (44) and level shifters (51-54) which are supplied with low logic amplitude clock signals. See Fig 8.

2. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art to to utilize Ishii's level shifters in Moriyama's display device. One would have been motivated that the level shifters can be used for desired application and increament of clock signals. The use of level shifter helps liquid crystal device function effectively as taught by Ishii.

Claim Rejections 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriyama et al. (USPN 6232945) in view of Ishii (USPN 6081131).

Regarding claims 1, 16 and 20, Moriyama teaches a shift register circuit containing multiple cascade-connected flip flops in synchronization with clock signals. See col. 2, lines 40-50. Moriyama teaches a display panel section (281) including multiple pixels arranged in a matrix form. Moriyama teaches scanning line driving circuit (293) with multiple scanning lines (Y1, Y2..Yn) and video signal line driving circuit (291) with multiple video signal lines. See Fig 1. Moriyama also teaches that the scanning line driving circuit in terms of voltage application at different timing (tsub0, tsub 1..tsub 4). See Fig 3 and col. 8, lines 12-53. Furthermore, Moriyama teaches the video signal line driving circuit that includes video signal selecting circuit (205) which

outputs video signals data including non-displayed data. See col. 6, lines 32-43, col. 7, lines 54-59, 65-67, col. 8, lines 1-2 and Fig 2. Moreover, Moriyama teaches the video signal driving circuit in terms of matrix wiring section (201) and logic circuit (202) that will enable the display data to be displayed on the pixels arranged on the (N-1)the line from the display area (502). See col. 8, lines 12-28 and Fig (1- 4). However, Moriyama does not teach about a level shifter for applying a clock signal and for increasing a voltage of a clock signal. On the other hand Ishii teaches a Liquid crystal device including level shifters (51, 52, 53, 54). See Fig 8. Ishii also teaches a logic amplitude level converter (10) including a voltage biasing means. See Fig 3, col. lines 44-50.

Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify Moriyama's display device to include Ishii's level shifters. One would have been motivated in view of the suggestion in Ishii that the level shifters can be used for desired application and increment of clock signals. The use of level shifters helps Liquid crystal device function more effectively as taught by Ishii.

Regarding claims 2-3, Moriyama teaches that when a pulse is inputted to the flip flop 22 sub1 from outside, the start pulse is transferred to the succeeding stage flip-flop 22 sub 2. See col. 15, lines 10-16.

Regarding claims 4-5 and 21, Moriyama teaches a reset circuit for outputting a signal for selecting a the scanning line based on the output of the flip-flop of the shift register. See col. 3, lines col. 3, lines 39-43.

Regarding claim 6, Moriyama teaches the input stage switching circuit (23) in terms of multiple flip-flops as well as pulse input and output. See col. 15, lines 7-18.

Regarding claims 7-9, 11-12, Ishii teaches a level shifter (2) obtaining an output clock signal,

V (out) through selector /offset circuits (1A, !B). See col. 1, lines 30-42 and Fig 11.

Regarding claim 10, Ishii teaches a level shifter (2) in terms of constant current source (4). See Fig 11.

Regarding claim 13, 22-25, Ishii teaches an output inverter (3) of an output-stage buffer circuit for buffering interactions in the input-output process. See col. 1, lines 40-43. Furthermore, Ishii teaches level shifter in connection with vertical shift register (44). See Fig 8.

Regarding claim 14, Ishii teaches a level shifter (53) with respect to horizontal clock signals (HCK1, HCK2). See Fig 8.

Regarding claim 15, Moriyama teaches a display device with 853 times 480 pixels. See Fig 14. Moriyama also teaches the input staging circuit (23) as it relates to the output of the flip flop 22 sub 107. See col. 15, lines 17-18.

Regarding claims 17-19, Moriyama teaches a display device as shown in Figure 1. See (293, 100, 121, 351) of Fig 1.

Conclusion

4. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to crystal park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Abbas Abdulselam

Examiner

Art Unit 2674